High Gain Soft-switching Bidirectional DC-DC Converters for Eco-friendly Vehicles

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Abstract—This paper proposes a non-isolated soft-switching bidirectional DC-DC converter suitable for high step-up and step-down applications. The proposed converter can achieve ZVS turn on of all switches and ZCS turn off of some switches in both CCM boost and buck operations. An optimized switching strategy is presented to minimize switch current rating and achieve soft-switching in wider range. An intermediate switching pattern is introduced to carry out seamless mode change. Experimental results from a 5kW prototype are provided to validate the proposed concept.

I. INTRODUCTION

In hybrid electric vehicles (HEV) the input voltage of the inverter has a tendency to increase in order to use high speed high power motor and improve the efficiency and power density of the inverter. For example, the input voltage has increased from 500V to 650V in 3rd generation PCU of Toyota Prius HEV where a Ni-MH battery of nominal voltage of 201.6V has been installed[1]. In the meantime the battery voltage is preferred to be low since parallel strings of storage batteries not only enhance the redundancy of the back-up system but also alleviate the problems associated with charge imbalance compared to series strings. Therefore, high efficiency bidirectional DC-DC converter (BDC) with high voltage gain is necessary in the aforementioned systems. The non-isolated BDC based on the half-bridge topology has a simple structure but should operate at high duty cycle to provide high step-up gain (greater than 4) when the battery voltage is low. Then, the boost diode must sustain a short pulse current with high amplitude, resulting in severe reverse recovery as well as high EMI problems. Using an extreme duty cycle may also lead to poor dynamic responses to line and load variations. Moreover, the switch should sustain high output voltage, and hence switch conduction losses resulting from the high on drop voltage of the high-voltage-rated switches are considerable. These make the conventional half-bridge topology inefficient in the applications where high voltage gain is required.

BDCs based on coupled or tapped inductors [2]-[5] can provide high output voltage without extreme duty cycle and yet reduce the switch voltage stress. In these coupled inductor converters, in general, the effort to overcome the problem associated with leakage inductor of the coupling inductor is non-trivial, and the capacity of the magnetic core should substantially be increased as the required output power is increased. Therefore, these topologies incorporating the coupling inductor are not suitable for high power applications. Also, the input current ripple is considerable due to the operation of coupling inductor.

The BDC using switched-capacitor converter cells could have more modular structure and higher power handling capability, but the required number of switches becomes high [6]-[8]. They are hard-switched, and high current pulse occurs since two capacitors with different voltages are connected in parallel at each switching instant. A major drawback of the switched-capacitor based converter is that ESR drop of the active and passive devices is considerable due to high number of series connected devices in the current path, resulting in reduced output voltage. This may restrict the power level to which the switched-capacitor converter can be applied.

Soft switched BDCs with a auxiliary circuit have been proposed to achieve ZVS or ZCS of main switches in both boost and buck modes of operations [9],[10]. The converter in [10] shows high efficiency despite of its circuit complexity. However, they are not suitable for applications where high voltage conversion ratio in both buck and boost operations is required. So far, the non-isolated BDC with high voltage gain that can be applied to high power level has rarely been proposed.

In this paper a new non-isolated BDC for high step-up/step down and high power applications is proposed. The optimized PWM switching technique for buck and boost operation and smooth mode transition is also presented. The proposed converter has the following advantages:

• High voltage gains for both boost and buck mode operations.
• Reduced voltage stresses of switches.
• ZVS turn-on of switches in CCM operation.
• Reduced energy volumes of passive components
• Seamless mode transition

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II. PROPOSED CONVERTER

Fig. 1 shows the circuit diagram of the proposed BDC. The proposed converter consists of a general buck/boost converter as the main circuit and an auxiliary circuit which includes capacitor $C_a$, inductor $L_a$ and two high voltage side (HVS) switches $S_3$ and $S_4$. The goal of control in this paper is to regulate the HVS voltage $V_H$ while allowing bidirectional power flow according to the direction of inductor current $I_L$.

A. Operating Principle

Assume that capacitances $C_1$, $C_2$ and $C_a$ are large enough so that voltages $V_{C_1}$, $V_{C_2}$ and $V_{Ca}$ across them are constant during the switching period $T_S$.

1) Boost Operation

Fig. 2 and Fig. 3 show key waveforms and operation states of the boost mode, respectively. In this mode, low voltage side (LVS) switches $S_1$ and $S_2$ are operated with asymmetrical complementary switching with duty cycles of $D$ and $1-D$, respectively, as shown in Fig. 2. In the mean time HVS switches $S_3$ and $S_4$ are turned on with delay times of $t_{d3}$ and $t_{d4}$, respectively. The operation of the proposed converter can be divided into five modes, as shown in Fig. 3.

Mode 1 ($t_0$ to $t_1$): This mode begins with turning off of $S_2$ and $S_4$. Then the body diodes of $S_1$ and $S_4$ are turned on. The gating signal for $S_1$ is applied with appropriate dead-time during this mode, and then $S_1$ could be turned on under ZVS condition. Inductor currents $i_L$ and $i_{La}$ start to increase and decrease, respectively, with the slopes determined by the following equations:

$$\frac{d}{dt}i_{L_f} = \frac{V_L}{L_f}$$

Fig. 1. Proposed high step-up soft-switched bidirectional dc-dc converter.

Fig. 2. Key waveforms of the proposed converter (boost mode).

Fig. 3. Operation states of the proposed converter (boost mode).


\[
\frac{d}{dt}i_{La} = \frac{V_{Ca} - V_{C1} - V_{C2}}{L_a}.
\]  

(2)

**Mode II** \(t_1 \sim t_2\) : When the increasing current \(i_{Lp}\) becomes greater than the decreasing current \(i_{La}\), current flowing through \(S_1\) is reversed, and the main channel of \(S_1\) conducts. This mode ends when the decreasing current \(i_{La}\) reaches to 0A. Note that switch \(S_4\) is also turned off under ZCS condition.

**Mode III** \(t_2 \sim t_3\) : At \(t_2\) current \(i_{La}\) is reversed and the body diode of \(S_3\) is turned on. For synchronous rectification with delay time of \(t_{d2}\), note that \(S_1\) is turned on under ZVS condition. Inductor current \(i_{La}\) linearly increases with the slope determined by the following equations:

\[
\frac{d}{dt}i_{La} = \frac{V_{Ca} - V_{C1}}{L_a}.
\]  

(3)

Both inductor currents \(i_{Lp}\) and \(i_{La}\) flow through switch \(S_1\).

**Mode IV** \(t_3 \sim t_4\) : At \(t_3\) switches \(S_1\) and \(S_3\) are turned off, and then body diodes of \(S_2\) and \(S_1\) are turned on. Both inductor currents \(i_{Lp}\) and \(i_{La}\) start to decrease with the slopes determined by the following equations:

\[
\frac{d}{dt}i_{Lp} = \frac{V_{La} - V_{C1}}{L_f}
\]  

(4)

\[
\frac{d}{dt}i_{La} = \frac{V_{Ca} - V_{C2}}{L_a}.
\]  

(5)

The gating signal for \(S_2\) is applied with appropriate dead-time during this mode, and then \(S_2\) could be turned on under ZVS condition. This mode ends when the decreasing current \(i_{La}\) reaches to 0A. Note that switch \(S_3\) is also turned off under ZCS condition.

**Mode V** \(t_4 \sim t_5\) : This mode begins when current \(i_{La}\) is reversed and the body diode of \(S_4\) is turned on. For synchronous rectification the gating signal for \(S_4\) can be applied after \(t_4\). Note that \(S_4\) is turned on under ZVS condition. Inductor current \(i_{La}\) linearly increases with the slope determined by the following equation:

\[
\frac{d}{dt}i_{La} = \frac{V_{Ca} - V_{C2}}{L_a}.
\]  

(6)

This is the end of one complete cycle.

2) **Buck Operation**

Fig. 4 and Fig. 5 show key waveforms and operation states of the buck mode, respectively. In this mode, HVS switches \(S_3\) and \(S_4\) are operated with asymmetrical complementary switching with duty cycles of \(D\) and \(1-D\), respectively, as shown in Fig. 4. In the mean time LVS switch \(S_2\) is turned on with delay time of \(t_{d2}\). The operation of the proposed converter can be divided into six modes, as shown in Fig. 5.

**Mode I** \(t_0 \sim t_1\) : This mode begins with turning off of switches \(S_2\) and \(S_3\). Then the body diodes of \(S_1\) and \(S_3\) are turned on after the parasitic capacitors of \(S_1\) and \(S_3\) are completely discharged. Inductor current \(i_{Lp}\) starts to decrease with the slope determined by equation (1).

**Mode II** \(t_1 \sim t_2\) : At \(t_1\) inductor current \(i_{Lp}\) starts to decrease with the slope determined by equation (3).

After appropriate dead-time switches \(S_1\) and \(S_3\) are turned on. The gate signal for \(S_1\) should be applied before reversal of current \(i_{Lp}\) for ZVS turn on. Note \(S_1\) is turned on without any delay for synchronous rectification. This mode ends when the decreasing current \(i_{La}\) reaches to 0A.

**Mode III** \(t_2 \sim t_3\) : At \(t_2\) inductor current \(i_{La}\) is reversed and starts increasing with slope determined by equation (2).

From equation (3) the positive peak value of \(i_{La}\) can be obtained as follows:

\[
I_{La+} = \frac{V_{Ca} - V_{C1}}{L_a} \cdot DT_s + V_{C2} \cdot \sqrt{2 \cdot C_{oss} \cdot \frac{La}{L_a}}.
\]  

(7)

**Mode IV** \(t_3 \sim t_4\) : Switches \(S_1\) and \(S_3\) are turned off at \(t_3\), and then body diodes of \(S_1\) and \(S_4\) are turned on. Inductor current \(i_{La}\) starts to decrease with the slope determined by equation (2).

Note that \(S_4\) could be turned on under ZVS condition if the gate signal for \(S_4\) is applied with appropriate dead-time before reversal of current \(i_{La}\). This mode ends when the decreasing
current $i_{La}$ reaches to 0A.

Mode V: When the increasing current $i_{La}$ becomes greater than the decreasing current $i_{Lf}$, body diode of S1 is turned off under ZCS condition. Then after parasitic capacitors of S1 and S2 are completely charged and discharged, respectively, the body diode of S2 is turned on and inductor currents $i_{La}$ and $i_{Lf}$ start to decrease and increase, respectively, with slopes determined by equations (6) and (4).

The negative peak value of $i_{La}$ is determined by the following equation:

$$I_{La}^- = I_{Lf}^- + \frac{\Delta I_{Lf}}{2} - \frac{V_{c1}}{\sqrt{L_a/(2 \cdot C_{oss})}}. \quad (8)$$

For ZVS turn on of S2 the gate signal for S2 should be applied before the decreasing current $i_{La}$ becomes smaller than the increasing current $i_{Lf}$.

Mode VI: At $t_5$ switch current $i_{S2}$ is reversed. Inductor currents $i_{La}$ and $i_{Lf}$ keep decreasing and increasing with slopes determined by equations (6) and (4), respectively. At the end of this mode S2 and S4 are turned off. This is the end of one complete cycle.

B. Voltage Conversion Ratio

The HVS voltage is given by the following equation:

$$V_{H} = \frac{2}{1-D_{eff}} \cdot V_L \quad (9)$$

where the effective duty is defined as follows (See Fig. 2):

$$D_{eff} = D - (d_3 + d_4) \quad (10)$$

where $d_3 + d_4$ means duty loss. The output voltage can also be expressed as follows:

$$V_{H} = \frac{2}{1-D} \cdot V_L - \Delta V \quad (11)$$

where $\Delta V$ is the voltage drop caused by the duty loss. From (9), (10) and (11) the voltage drop $\Delta V$ can be obtained as follows:

$$\Delta V = \frac{2 \cdot V_L \cdot (d_3 + d_4)}{(1-D)(1-D+1)} \quad (12)$$

Voltage $V_{c1}$ that is same as output voltage of the general boost converter can be expressed as follows:

$$V_{c1} = \frac{1}{1-D} \cdot V_L \quad (13)$$

By applying volt-second principle to inductor $L_a$, we can obtain the minimum delay times for ZVS turn on of S2 and S4 by the following equations:

$$d_3 T_S = \frac{I_{La} \cdot L_a}{V_{c1}} \quad (14)$$

$$d_4 T_S = \frac{I_{La} \cdot L_a}{V_{c1}} \quad (15)$$

Since the average value of switch currents $i_{S3}$ and $i_{S4}$ is the same as that of HVS current $I_{H} = \frac{V_H \cdot R_{LH}}{2}$ and the difference in duty losses $d_3$ and $d_4$ are much smaller than duty cycle $D$, positive and negative peak values of the inductor current $i_{La}$ can be approximated, respectively, by
\[ I_{La} = \frac{2}{1-D} \frac{V_{In}}{R_{hi}} T_s \] (16)

\[ I_{Ld} = \frac{2}{D} \frac{V_{In}}{R_{hi}} T_s \] (17)

The actual delay times for S3 and S4, \( t_{\alpha} \) and \( t_{\beta} \), are determined, respectively, as follows:
\[ t_{\alpha} = d_t T_s + \text{dead-time} \] (18)
\[ t_{\beta} = d_t T_s + \text{dead-time} \] (19)

From (9), (10), (13), (14) and (15) the voltage gain can be obtained as follows:
\[ V_{hi} = \frac{\sqrt{\alpha^2 (1-D)^2 + 4\alpha\beta - \alpha(1-D)}}{\beta} \] (20)

where \( \alpha = DR_{hi} \) and \( \beta = 4L_u \).

Using (20) the voltage gain of the proposed converter is plotted as shown in Fig. 6.

**C. Mode Change Strategy**

The optimized switching patterns for boost and buck operations are different as we can see from Fig. 7(a) and (c). In this section a mode change strategy is proposed for seamless transfer from buck mode to boost mode, and vice versa. In order to carry out seamless transfer during mode change an intermediate switching pattern (See Fig. 7(b)) is inserted between the two switching patterns for boost and buck modes. The switching sequence for transfer from boost mode to buck mode is Pattern1 \( \rightarrow \) Pattern2 \( \rightarrow \) Pattern3. The switching sequence for transfer from buck mode to boost mode is Pattern3 \( \rightarrow \) Pattern2 \( \rightarrow \) Pattern1. Fig. 8 and Fig. 9 show the switching sequence and control block diagram for the proposed BDC, respectively. The moment at which the switching pattern is changed is determined by comparing the instantaneous average value \( I_{Lf,avg} \) of the inductor current to the preset values of \( I_{Lf,upper} \) or \( I_{Lf,lower} \).
III. EXPERIMENTAL RESULTS

The interleaving technique can be applied to reduce the size of passive components and current stresses. A 5kW prototype of the two-phase interleaved version of the proposed converter shown in Fig. 10 was built according to the following specification:

- $P_o = 5\text{kW}$
- $V_H = 400\text{V}$
- $V_L = 72\text{V}$
- $f_s = 20\text{kHz}$
- $L_s = 4\mu\text{H}$
- $C_s = C_1 = C_2 = 30\mu\text{F}$

Both LVS and HVS switches are implemented with IXFN100N50P(500V, 90A, and 49mΩ) MOSFET. The nominal duty cycle of 0.64 was used to achieve voltage gain of 5.5 in both buck and boost modes of operation. The actual delay times $t_{d2}$, $t_{d3}$ and $t_{d4}$ were chosen to be 1500ns, 1500ns and 1200ns, respectively. The pre-set values $I_{fupper}$ and $I_{flower}$ for mode change were used as 1.5A and -1A, respectively. Experimental waveforms of mode change are also shown in Fig. 11. It is seen that there are no transients caused by change of switching patterns during the mode change. Experimental waveforms of the proposed converter for boost and buck operations are shown in Figs. 12 and 13, respectively. Figs. 12 (a) to (d) show voltage and current waveforms of switches S1 to S4 in boost mode. Figs. 13 (a) to (d) show voltage and current waveforms of switches S1 to S4 in buck mode. It can be seen that all switches are turned on with ZVS in both operations. The measured efficiency is shown in Fig. 14. The efficiency was measured by YOKOGAWA WT3000. The maximum efficiency in boost mode and buck mode is 97.3% at 1kW and 97.2% at 2kW, respectively.

IV. CONCLUSION

In this paper a non-isolated soft switching BDC has been proposed for high voltage gain and high power applications.
The proposed converter can achieve ZVS turn on of all switches and ZCS turn of some switches in both boost and buck operations. An optimized switching sequence is presented along with an intermediate switching pattern to carry out seamless mode change. A 5kW prototype of the proposed converter has been built and tested to verify the validity of the proposed operation. A nominal duty cycle of 0.64 was used to achieve voltage gain of 5.5 in the both buck and boost modes of operation.

 REFERENCES